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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,943	03/01/2002	Kazuya Kawakami	843.41231X00	8260

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EXAMINER
PERALTA, GINETTE

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,943	KAWAKAMI ET AL.	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *14-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-13 in Paper No. 4 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Theriault et al. (U. S. Pat. 6,530,732 B1) in view of Farber et al. (U. S. Pat. 6,232,134 B1) and Yasuyuki.

Theriault et al. discloses a system of manufacturing a semiconductor integrated circuit device performed in a semiconductor manufacturing apparatus having a plurality of chambers that comprises processing a semiconductor wafer in a first processing chamber; transporting the semiconductor wafer to a second chamber and performing a second process to the semiconductor wafer.

Theriault et al. discloses the claimed invention with the exception of obtaining a flat entire image of the semiconductor wafer after performing the first process, determining the condition of the wafer by examining the flat entire image, and

transporting the semiconductor wafer to the second chamber if the semiconductor wafer is determined to be in proper condition or stopping the operation if the wafer is determined to be in improper condition.

Farber et al. discloses a method of manufacturing a semiconductor integrated circuit device performed in a semiconductor manufacturing apparatus having a plurality of chambers (col. 10, ll. 55-67), wherein the method comprises obtaining a flat entire image of a semiconductor wafer after performing a first process to the semiconductor wafer in a first chamber and before performing a second process to the semiconductor wafer in a second chamber; determining the condition of the

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(col. 4, ll. 39-51) by comparing a flat entire image of a good semiconductor wafer recorded in advance and the flat entire image of the semiconductor wafer; and making adjustment depending on whether the semiconductor wafer is found to be in proper or improper condition, wherein the examining of the flat entire image of the semiconductor wafer and using the information to determine the condition of the wafer between process steps is for the disclosed intended purpose of monitoring performance of processing steps in a manner that require less manual interaction, produces more accurate results, and which can be performed in a fast and efficient manner such that more frequent monitoring can be performed in a cost effective manner.

Yasuyuki discloses a method of manufacturing a semiconductor integrated circuit device that comprises obtaining an entire image of a wafer after performing a

first process to the semiconductor wafer; determining the condition of the semiconductor wafer by examining the entire image; and stopping the operation of the semiconductor manufacturing apparatus when the semiconductor wafer is in improper condition, wherein Yasuyuki removes the semiconductor wafer determined to be in improper condition automatically in order to remove the semiconductor wafers that are not suitable to continue in to the following processing steps.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to obtain a flat entire image of a semiconductor wafer after a first processing step and prior to a second processing step, to determine the suitability

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semiconductor wafer if the semiconductor wafer is determined to be in improper condition for the purposes of Farber et al. and Yasuyuki of monitoring performance of processing steps in a manner that require less manual interaction, produces more accurate results, and which can be performed in a fast and efficient manner such that more frequent monitoring can be performed in a cost effective manner; and in order to remove the semiconductor wafers that are not suitable to continue in to the following processing steps.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703)305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

GP

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800